

Features of Decision Support's Program at Choice of Tests Optimized Sequence for Semiconductors Memory Diagnosing

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Abstract – a method, which allows decreasing calculations works labour intensiveness at the choice of pareto-optimum tests for semiconductors storage devices diagnosing is offered. This method is realized in the program *Optimal-test*, which allows decreasing the duration of memory's microcircuits testing without worsening of their quality.

Index Terms – diagnosing, microcircuit, memory, test.

I. INTRODUCTION

At mastering mass-produced storages devices it is necessary to choose a control-diagnostic equipment and set of effective tests to include them in the program of tests. Acquisition of control-diagnostic facilities is carried out on the basis of analysis of technical descriptions and determination of their conforming to produced requirements. First task behave to the cleanly technical tasks, its decision does not require considerable efforts. Considerable difficulties arise up at the choice of effective diagnostic tests and modes task of tests of semiconductor memory's wares [1-3].

For providing of the production plan fulfilling and issue of high quality wares, it is necessary to apply the optimized sequence of tests, which provide achieving high efficiency of diagnosing at the limited resources of productions of time and equipment. For providing of operative adjustment of the program of tests a programmatic facilities development of decision-making support is required.

To improve the wares quality it is necessary to multiply the duration of the test diagnosing, that will multiply the cost of wares and diminishes the Sales Quantity, and the circle of causal-effective connections is locked. Every firm decides independently, what time of the test diagnosing will be for it optimum and will allow to attain the set quality of wares.

Providing of possible economic level of memory's microcircuit and modules diagnosing of memory is one of tasks, which must be decided by managers of technical quality control departments of firms of designing, making and exploiting facilities of the computing engineering,

which are intended for the informative and control systems construction.

For diminishing of labour intensiveness of solving of this task, a special methods, algorithms and programs development is needed, which allow to use wide possibilities of the modern computing engineering for sorting of data array, describing a priori properties of the applied tests.

In the known algorithms of data sorting the arrays of integer or real numbers are processed and a new well-organized by ascending array of numbers is formed as a result [4]. However these algorithms after implementation of sorting operation do not allow identifying property, which objects estimate well-organized cells of got array.

The purpose of this paper is development of algorithm and method of choice of the optimized set of tests, providing combination of high efficiency with the possible economic level of memory's microcircuit and modules diagnosing of memory.

II. MATHEMATICAL MODEL AND SOLVING OF RESEARCH TASK

At the choice of the tests optimized sequence for memory's microcircuits and modules diagnosing, it is necessary to take into account, that their diagnostic properties are unclear certain, and tests are offered, which their detailed algorithmic description is not expounded even. In the conditions of presence of a priori unclear information about diagnostic properties of tests it is expedient to apply the method of choice of pareto-optimum tests, in which criterion of tests quality determined by skilled specialists in area of semiconductors storages devices diagnosing.

The most essential criterion for the estimation of tests properties is their ability to find out most widely showing up refusals of memory's cells, decoders of address, reading amplifiers of charges renewal charts in memorizing condensers and other.

These properties of tests are estimated by probabilities of finding out the refusals of the set types and measured by real numbers in a range from 0 to 1 and therefore they compared easily.

The vector of comparison $S_i^{\vartheta\mu}$ of tests properties ϑ and μ on probably of finding out the refusal of i -type is determined by the following expression:

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$$S_i^{\mathcal{G}\mu} = 1, \text{ if } q_{i_i}^{\mathcal{G}} > q_{i_i}^{\mu};$$

$$S_i^{\mathcal{G}\mu} = 0, \text{ if } q_{i_i}^{\mathcal{G}} = q_{i_i}^{\mu};$$

$$S_i^{\mathcal{G}\mu} = -1, \text{ if } q_{i_i}^{\mathcal{G}} < q_{i_i}^{\mu},$$

where $q_{i_i}^{\mu}, q_{i_i}^{\mathcal{G}}$ – probabilities of finding out the refusals of i type of tests \mathcal{G} and μ accordingly.

For every criterion it is possible to get its mean value by the formula: $E_{mid}^j = \sum_{i=1}^n E_{ij} / n$

Then the rationed value of estimation C_{ij} of properties of i - test on finding out the malfunction of j -type it is possible to get through this expression:

$$C_{ij} = 1, \text{ if } E_{ij} > E_{mid}^j;$$

$$C_{ij} = 0, \text{ if } E_{ij} = E_{mid}^j;$$

$$C_{ij} = -1, \text{ if } E_{ij} < E_{mid}^j.$$

An important factor is also time of tests implementation, which can depending on complication of test be measured in microseconds, hours and even to achieve astronomical values. Logically, that tests of which duration do not accord the economic feasibilities of production or exploitation conditions $t_j > t_{max}$, it is necessary to exclude from the examined great number.

For the remaining group, it is necessary to ration the value of parameter testing time and for every test to get the vector of estimation of properties on execution time in according to expression: $S_i^j = (\sum_{j=1}^n t_j / n) / t_j$, where

S_i^j – estimation of properties of j -type test at implementations times; n – Number of tests; t_j – time of implementation of j -test.

Estimations for m criteria and n tests are presented in table. 1.

TABLE 1
ESTIMATIONS FOR TESTS PROPERTIES

Test Name	Estimations for criteria's				
	1	2	3	...	m
Test 1	S_{11}	S_{12}	S_{13}	...	S_{1m}
Test 2	S_{21}	S_{22}	S_{23}	...	S_{2m}
		...			
Test n	S_{n1}	S_{n2}	S_{n3}	...	S_{nm}

Generalized estimation S_{sum}^i for every test it is possible to get by the formula: $S_{sum}^i = \sum_{j=1}^m s_{ij}$.

Thus, the task of choice of the optimized tests set is taken to ranging of tests, or to the sorting by their generalized estimations ascending.

III. FEATURES OF THE PROGRAM OF THE OPTIMIZED TESTS SEQUENCE CHOICE

For the programming realization of researched task it is suggested to use the determined by the user structured information with the following kind:

```

Typedef struct
{
    Int Estimation;
    Int Number;
    Char Name [12];
} DATA;

```

As input data to the computer's memory the array of the structured data, containing probabilities of exposure of refusals and tests names, is added.

For sorting of data array it is suggested to use the algorithm of "bubble", where records with the "easy" values of the key field emerge upwards like a bubble. With the purpose of diminishing of steps of algorithm a special flag, allowed comparison of array cells, is entered, and in the beginning this value of this flag will be one.

After activation of comparison operation of a flag with a value zero, and then in pairs compare array cells: first with the second, second with the third and etc, simultaneously assort them. If transposition of elements was carried out, a value is again the flag appropriates a value one and a new cycle of elements sorting begins. If a flag was not set in the one state, it means that there is nothing to assort and a process is stopped.

IV. PRACTICAL RESULTS OF RESEARCH

Diagnostic experiments were executed at two different values of power supply tension: high tension (HVcc) and low tension (LVcc). At HVcc in 1545 microcircuits were discovered disrepairs, from them 1343 microcircuits the defects were detected by all tests and only in 202 microcircuits the defects were discovered only by one or a few tests [5].

For implementation of diagnostic experiments the tests were used, of which execution time for the memory's microcircuits of different capacity is resulted in tabl1.

Probabilities of finding out refusals in the microcircuits of memory through the sets of tests of consisting of combinations from two tests calculated on formulas:

$$\forall i, i = \overline{1, n}, q_i = \frac{m_i}{m_s}, \forall i, j = \overline{1, n}, i \neq j, q_{ij} = \frac{m_i \cup m_j}{m_s},$$

where m_i, m_j – an amount of microcircuits, discovered by the tests of i, j accordingly; m_s – common amount of defective microcircuits.

Implementation time of the most widespread tests is resulted in table. 2. Time of implementation of different tests can be measured by seconds and can achieve a few days even.

If not to apply measures on optimization of tests set, so the time of arbitrary sequence of tests performance can reach great values and thus the cost of memory's microcircuits will grow sharply.

TABLE 2
IMPLEMENTATION TIME OF EXAMINED TESTS

№	Test Name	Formula	Time while $t_c = 5$ nsec and memory's capacity Mb, sec				
			1	4	16	64	256
1	WalkRow	$8n+2nC$	10.779	86.067	687.866	5500	43990
2	WalkColumn	$8n+2nR$	10.779	86.067	687.866	5500	43990
3	GalRow	$6n+4nC$	21.508	171.925	1375	11000	87970
4	GalColumn	$6n+4nR$	21.506	171.925	1375	11000	87970
5	Hammer	$49n$	0.257	1.028	4.11	16.442	65.767
6	March SL	$41n$	0.215	0.86	3.439	13.757	55.029
7	March RAW	$26n$	0.136	0.545	2.181	8.724	34.897
8	March SS	$22n$	0.115	0.461	1.845	7.382	29.528
9	March G	$23n$	0.121	0.482	1.929	7.718	30.87
10	March SR	$14n$	0.073	0.294	1.174	4.698	18.79
11	PMOVI	$13n$	0.068	0.273	1.091	4.362	17.448
12	March C	$10n$	0.052	0.21	0.839	3.355	13.422
13	MATS++	$6n$	0.031	0.126	0.503	2.013	8.053
14	MATS+	$5n$	0.026	0.105	0.419	1.678	6.711
15	Scan	$4n$	0.021	0.084	0.336	1.342	5.369

Results of choice of Paret-optimum sequence of tests, got on the offered algorithm, at HVcc resulted on a fig. 1.

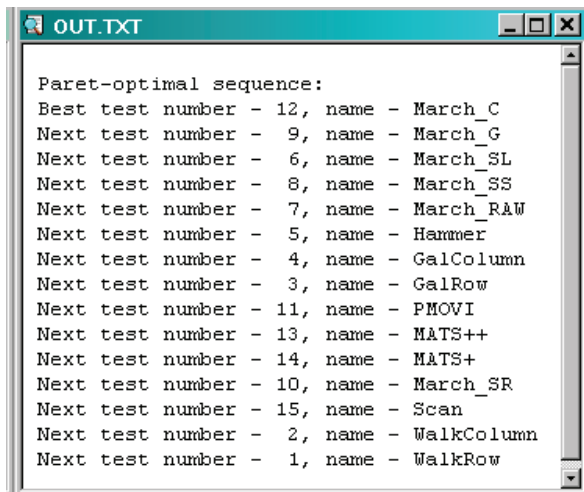


Fig. 1. Paret-optimum sequence of tests at HVcc

By results of experimental researches it is established, that 6 tests from the optimized set find out all defects of the given microcircuits, therefore the application of other tests is inexpedient.

The graphs of change duration of memory's microcircuits diagnosing are with a capacity 4 Mb at time of access cycle, equal 5 nsec at HVcc for the arbitrary sequence of tests and optimized sequence resulted on a fig. 2.

Implementation of 6 tests time from an arbitrary set of tests is 345,675 sec and for 6 tests from the optimized sequence – only 3,586 sec.

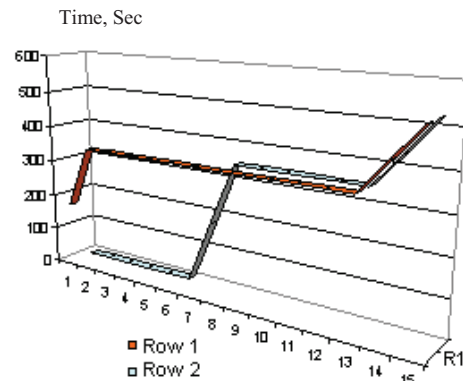


Fig. 2. Duration of diagnosing for the different sets of tests:
Row 1 - for the arbitrary sequence of tests;
Row 2 - for the optimized sequence

The histogram of duration of diagnosing for 6 tests from different sets is resulted on a fig. 3.

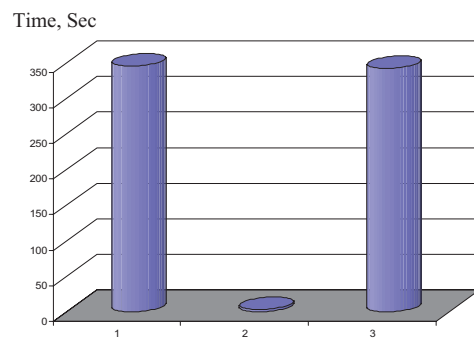


Fig. 3. Duration of diagnosing for different sets from 6 tests:
Column 1 – for the arbitrary sequence of tests; Column 2 – for the optimized sequence; Column 3 – economy of time.

As a result of analysis of this histogram, it is possible to do a conclusion, that the economy of time at application of the optimized set of tests makes 342,089 sec.

The results of choice of Paret-optimum sequence of tests at LVcc are resulted on a fig. 4.

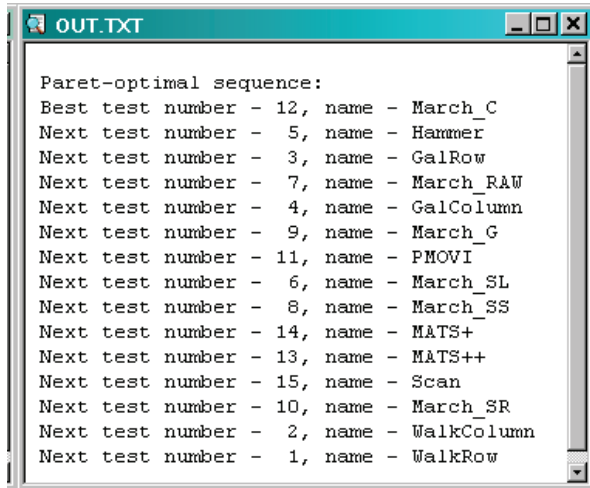


Fig. 4. Paret-optimum sequence of tests at LVcc

The graphs of change duration of memory's microcircuits diagnosing are with a capacity 4 Mb at time of access cycle, equal 5 nsec at LVcc for the arbitrary sequence of tests and optimized sequence resulted on a fig. 5.

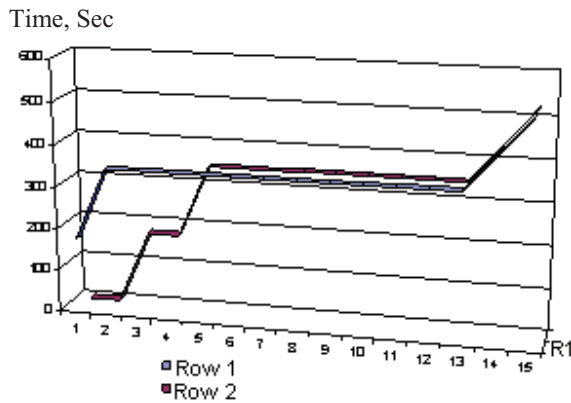


Fig. 5. Duration of diagnosing for the different sets of tests:
Row 1 – for the arbitrary sequence of tests;
Row 2 – for the optimized sequence

The obtained results show that for the different values of tensions of power supplies it is necessary to apply the different sets of tests, providing most economic expenses on conducting of the test diagnosing.

For two combinations of power supply tension: HVcc and LVcc time of diagnosing through 6 tests for the arbitrary sequence of tests is 691, 35 sec (see fig. 6), and for the optimized sequence of tests only 349,701 sec. Thus, the economy of time due of use of Optimal-test program is about 50%.

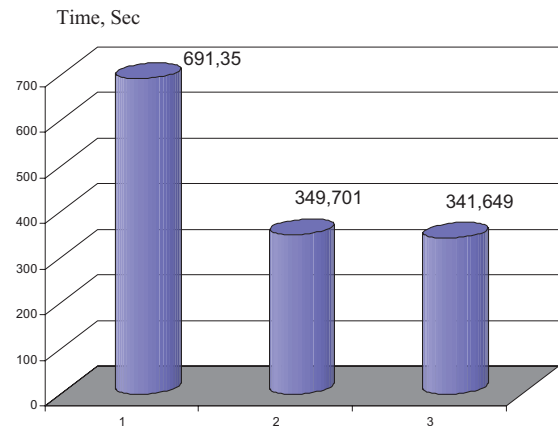


Fig. 6. Histogram of duration of tests:
First column – execution time of 6 tests from an unoptimized set,
Second – execution time of 6 tests from an optimized set,
Third – economy of time

V. CONCLUSION

The offered method and program allow decreasing labour intensiveness of calculations works at the choice of Paret-optimum tests for diagnosing of semiconductor storages devices. Application of the program Optimal-test will allow reducing expenses on implementation of the test diagnosing of storage devices and decrease their prime price.

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